A1

thickness of about 6000 Å. In an alternate embodiment, field oxide 402 can be replaced with a shallow trench isolation (STI) structure.

A2

[0038] Openings 409-411 also define the diffusion bit lines of array 100. More specifically, openings 409, 410 and 411 define the locations of diffusion bit lines 131, 132 and 133, respectively. After the above-described etching steps are completed, high angle implants are performed through openings 409-411. More specifically, a P-type impurity, such as boron, is implanted through openings 409-411 at high angles with respect to the upper surface of semiconductor substrate 401, such that the dopant extends under the edges of photoresist mask 408. In accordance with one embodiment of the present invention, the high angle implants are performed by implanting P-type impurities with a dopant density in the range of $1x10^{13}$ to $5x10^{13}$ ions/cm^2, and an implantation energy in the range of 40 to 100 KeV. In a particular embodiment, the high angle implants are performed with a dopant density of about $2.2x10^{13}$ ions/cm^2 and an implantation energy of about 25 KeV. In one embodiment, the high angle implants are performed at angles in the range of 15 to 45 degrees from the vertical axis of Fig. 8, which extends perpendicular to the upper surface of substrate 401. In the described embodiment, the high angle implants are performed at angles approximately 25 degrees from the vertical axis of Fig. 8. The implanted boron serves to adjust the threshold voltages of NVM transistors 101-104. The implanted p-type impurities are illustrated as regions 412-414 in Fig. 8. In an alternate embodiment, the p-type impurities can be implanted along the vertical axis of Fig. 8. Note that in the described example, the pocket implant

A2

(and other process features) are less critical than in the NVM transistor 10 of Figs. 1 and 2, because a simpler process technology is being used in the present invention.

A3

[0040] After performing the high angle implants, an N-type impurity, such as arsenic, is implanted through openings 409-411 of photoresist mask 408. In one embodiment, arsenic is implanted with a dopant density in the range of $1x10^{15}$ to $1x10^{16}$ ions/cm^2 and an implantation energy in the range of 30 to 100 KeV. In a particular embodiment, arsenic is implanted with a dopant density of about $3x10^{15}$ ions/cm^2 and an implantation energy of about 60 KeV. The implanted N-type impurities are illustrated as regions 422-424 in Fig. 9.

A4

[0044] After the polycide etch is completed, the photoresist mask is stripped and a tungsten silicide anneal is then performed at 900°C with low oxygen flow. (This anneal adheres the tungsten silicide to the underlying polysilicon and is part of the activation of the impurities in the buried diffusion bit lines 432-434). A boron implant is then performed to prevent current leakage between diffusion bit lines at the locations between adjacent gates electrodes in the fieldless array. This boron implant is a blanket implant, with no mask protection provided on the wafer. In one embodiment, boron is implanted at a dopant density in the range of $1x10^{12}$ to $6x10^{12}$ ions/cm^2 and an energy in the range of 20 to 60 KeV. In a particular embodiment, boron is implanted at a dopant density of about $3x10^{12}$ ions/cm^2 and an energy of about 30 KeV.

[0045] Fig. 12 is a top view of NVM transistors 101-104. NVM transistors 101-102 are labeled with the reference numbers described above in Figs. 4-11. Each of NVM transistors 101-104 has a horizontal dimension of 0.72 microns (between the centers of the adjacent diffusion bit lines), and a vertical dimension of 0.5 microns. These dimensions are shown on NVM transistor 104 in Fig. 12. The area of each NVM transistor is therefore 0.36 μ^2, with a per bit area of 0.18 μ^2.

A4

A5

Page 22, on the line after "CLAIMS", add --"I Claim:"--

IN THE CLAIMS

Cancel Claims 7-8 and 11-17.

Re-write Claim 1 as follows:

A6 Sub B1

1. (**Amended**) A two-bit non-volatile memory transistor comprising:

a semiconductor region having a first conductivity type;

a first source/drain region located in the semiconductor region, the first source/drain region having a second conductivity type, opposite the first conductivity type;

a second source/drain region located in the semiconductor region, the second source/drain region having the second conductivity type, wherein a channel region of the first conductivity type is located between the first and second source/drain regions;